CLAIMS

What is claimed is:

1. A memory, comprising:

a first magnetic memory element;

a first group of conductors magnetically coupled to the first magnetic memory element;

a second magnetic memory element; and

a second group of conductors magnetically coupled to the second magnetic memory element;

wherein the second memory element is substantially vertical to the first memory element, and the first and second group of conductors have at least one conductor in common.

2. The memory of claim 1, wherein the magnetic memory elements are capable of having their magnetic orientation adjusted by the common conductor.

3. The memory of claim 2, wherein power required to change magnetic orientation of the magnetic memory elements is dependant on the number of conductors, and wherein the number of conductors used for writing data to the memory elements is three or less.

4. The memory of claim 2, wherein the memory elements are written to a digital state by inducing current in the common conductor, and then the memory elements are selectively written to opposite digital states by inducing a current in the common conductor and inducing a current in a conductor that is not common to the memory elements.

5. The memory of claim 2, wherein the orientation of the magnetic memory elements are adjusted independently.

6. The memory of claim 1, wherein the magnetic memory elements further comprise hard axis magnetization thresholds that are altered.

7. The memory of claim 1, wherein the magnetic orientation of the memory elements are sensed while current flows in the common conductor.

8. The memory of claim 7, wherein read and write operations are performed simultaneously.

9. The memory of claim 1, wherein the common conductor is between the memory elements.

10. A method, comprising:

monitoring a plurality of memory elements, wherein the memory elements are substantially vertical;

providing a magnetic field to the memory elements using a conductor that is magnetically coupled to at least two memory elements; and

determining a digital state by monitoring the memory elements while the magnetic field is switched.

11. The method of claim 10, wherein monitoring comprises measuring the resistance of the memory element.

12. The method of claim 10, wherein monitoring comprises measuring the rate of change of the resistance of the memory element.

13. The method of claim 10, wherein the original magnetic orientation of the memory elements is not changed by the provided magnetic field.

14. A computer, comprising:

a processor;

a bridge logic device coupled to said processor;

a memory coupled to the processor, comprising:

a plurality of magnetic memory elements that exist on separate planes; and

a conductor magnetically coupled to the memory elements that are on separate planes.

15. The memory of claim 14, wherein the memory elements further comprise digital states, and wherein the conductor is used to modify the digital states of the plurality of magnetic memory elements.

16. The memory of claim 15, wherein the conductor provides independent control of the digital state of the memory elements.

17. A method, comprising:

providing a common conductor to a plurality of memory elements, wherein the common conductor magnetically couples to the memory elements;

inducing a magnetic field by flowing a current in the common conductor; and

altering the digital state of the memory elements using the induced magnetic field;

wherein the memory elements are not part of the same plane.

18. The method of claim 17, wherein power consumed by the memory elements is reduced.

19. The method of claim 17, further comprising monitoring the resistance of the memory elements while altering the digital state of the memory elements.

20. A computer, comprising:

a processor;

a bridge logic device coupled to said processor;

a means for storing information that is coupled to the processor, wherein the means for storing information comprises:

a first magnetic memory element;

a second magnetic memory element vertically stacked above the first magnetic memory elements; and

a conductor coupled to both the first and second magnetic memory elements, wherein the conductor is adapted to switch a magnetic orientation of the first magnetic memory element, the second magnetic memory element and both the first and second magnetic memory elements.